

REMARKS

Claims 1-53 are pending. By this amendment, claims 1 and 11 are amended.

The Office Action rejects claims 1-14 under the judicially created doctrine of obviousness-type double patenting over claim of applications 10/614,859, 10/614,860, 10/614,862, 10/614,863 and 10/614,864. It is submitted that this rejection for each of these applications should be provisional, until one of the applications is otherwise ready to issue. That application should then be allowed to issue, and the double patenting rejection, if still in affect, should be made non-provisional, and applicants will then consider whether to submit a terminal disclaimer.

The Office Action objects to claim 11 due to an informality. Claim 11 has been amended as suggested and withdrawal of the objection is requested.

The Office Action rejects claims 1-53 under 35 USC 103 over O'Brien (US Pat. 5,247,638 in view of Stallmo (US Pat. 5,526,482). This rejection is respectfully traversed.

Independent claim 1 of the application recites a storage device that includes a "first processor controlling transfer of data between the channel unit and the plurality of cache units" and a "second processor controlling transfer of data between the plurality of control units and the plurality of cache units". In addition, the other elements recited allow "the transfer of the data between the channel unit and the cache unit" and the "transfer of data between the plurality of control units and the cache units". This allows transfer of the data between different recited units in parallel. Accordingly, both the process of reading/writing data related to the host computer from/to the cache unit and the process of reading/writing data between the cache unit and the disk device can be executed efficiently.

In contrast, as shown in Fig. 2 and so on of O'Brien, transfer of data in O'Brien between the multipath storage director 110 and the cache 113 and the transfer of data between the cache 113 and the cluster control 111 or the disk drive manager 102 are controlled only by the processor IUP204 by using the control bus 206-C. O'Brien does not disclose or suggest the

“first processor controlling transfer of data between said channel unit and said plurality of cache units”, or the “second processor controlling transfer of data between one or more of said plurality of control units and said plurality of cache units” as required by claim 1.

Stallmo does not solve these deficiencies. In Stallmo, only the memory control unit 2 is disposed among the host computer 1, the caches 8 and 9 and the external memory unit 3 to transfer data. So Stallmo does not disclose or suggest the “first processor controlling transfer of data between said channel unit and said plurality of cache units”, or the “second processor controlling transfer of data between one or more of said plurality of control units and said plurality of cache units” as required by claim 1. Stallmo also does not disclose the “channel unit” or the “control unit” as recited in claim 1.

Because neither of the applied references disclose or suggest the “first processor controlling transfer of data between said channel unit and said plurality of cache units”, or the “second processor controlling transfer of data between one or more of said plurality of control units and said plurality of cache units” as required by claim 1, even if combined, the applied references would not recite in the storage device of claim 1.

Accordingly, claim 1 and all claims dependent therefrom would not have been obvious over the applied references. Withdrawal of the rejection is requested.


For the above reasons, reconsideration of the rejections and an indication of allowable subject matter is requested. Should there be any questions, the Examiner is invited to telephone the undersigned.

The Commissioner is authorized to charge fees for this matter regarding 37 CFR §1.16,

PATENT
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§1.17 and §1.136 to Kenyon & Kenyon Deposit Account No. 11-0600.

Respectfully submitted,



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